WHAT IS CLAIMED IS:

1. A method for testing routing resources for control signals on a programmable integrated circuit (IC), the method comprising:

automatically generating test paths on the programmable IC, each test path including routing resources that route the control signals, a logic gate, and a dedicated test register, wherein the test register is not used in a user mode of the programmable IC;

applying test vectors to the routing resources for the control signals;

performing a logic function on the test vectors using the logic gate to generate test output values;

sequentially storing the test output values in the dedicated test register; and

comparing the test output values to expected values to isolate defects in the routing resources.

2. The method according to claim 1 wherein the routing resources are programmable interconnect resources that route clock signals.

3. The method according to claim 1 wherein the routing resources are programmable interconnect resources that route clear signals.

4. The method according to claim 1 wherein the routing resources are programmable interconnect resources that route clock enable signals.

5. The method according to claim 1 further comprising:

decoupling the control signals from functional registers on the IC.

6. The method according to claim 1 wherein each of the test paths begins at a source register.

7. The method according to claim 1 wherein each of the test paths begins at a clock pin.

8. The method according to claim 1 wherein the logic gate is an XOR gate.

9. The method according to claim 1 wherein the logic gate is a multiplexer.

10. The method according to claim 1 wherein the programmable IC is a field programmable gate array.

11. The method according to claim 1 further comprising:

coupling the control signals to the functional registers when the programmable IC is operated during a user mode.

12. A programmable integrated circuit comprising:

routing resources for routing control signals on the programmable integrated circuit;

a logic gate coupled to receive the control signals from the routing resources that generates output test values during a test mode;

a dedicated test register for sequentially storing the output test values during the test mode, wherein the dedicated test register is not operated during a user mode; and

an enable circuit that decouples the control signals from functional registers during the test mode and that couples the control signals to the functional registers during a user mode.

13. The method according to claim 12 wherein the routing resources are programmable interconnect resources that route clock signals.

14. The method according to claim 12 wherein the routing resources are programmable interconnect resources that route clear signals.

15. The method according to claim 12 wherein the routing resources are programmable interconnect resources that route clock enable signals.

16. The programmable integrated circuit of claim 12 wherein the logic gate is an XOR gate.

17. The programmable integrated circuit of claim 12 wherein the functional registers are located in logic elements on a field programmable gate array.

18. The programmable integrated circuit of claim 12 wherein the control signals are generated by logic elements on the programmable integrated circuit.

19. The programmable integrated circuit of claim 12 wherein the programmable integrated circuit is part of a digital system that includes a processor, memory and an I/O unit.

20. The programmable integrated circuit of claim 12 wherein the logic gate is a multiplexer.